USN

15EC32

Third Semester B.E. Degree Examination, June/July 2018

Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive an expression for A_V, Z_i and Z_0 for CE–fixed bias using r_e-equivalent model. **(08 Marks)**

b. Define h-parameters and derive h-parameters model of CE-BJT. **(08Marks)**

OR

2 a. For the emitter-follower network of Fig.Q2(a). Determine : i) r_e ii) Z_i iii) Z_0 iv) A_V. **(08 Marks)**

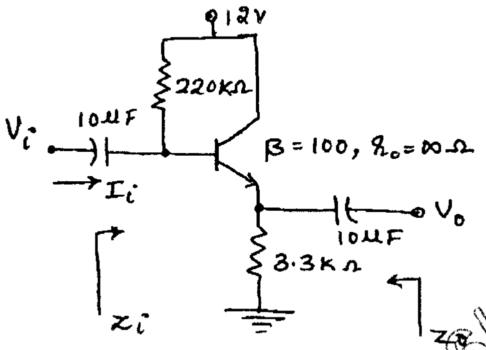

Fig.Q2(a)

b. With a neat circuit explain the high frequency transistor small-signal AC equivalent circuit. **(08 Marks)**

Module-2

3 a. Briefly explain the construction, operation and characteristics of n-channel D-type MOSFET. **(08 Marks)**

b. The fixed-bias configuration of Fig.Q3(b) has an operating point defined by $V_{GS_Q} = -2V$ and $I_{D_Q} = 5.625mA$, with $I_{DSS} = 10mA$ and $V_P = -8V$.

Determine : i) g_m ii) r_d iii) Z_i iv) Z_0 v) A_V. **(08 Marks)**

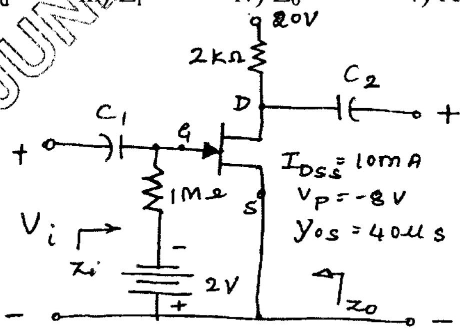

Fig.Q3(b)

OR

4 a. Explain the small signal model of the FET. (06 Marks)
b. Compare JFET and MOSFET. (03 Marks)
c. Draw the JFET common drain configuration circuit. Drive Z_i, Z_0 and A_V using small signal model. (07 Marks)

Module-3

5 a. The input power to a device is 10,000W at a voltage of 1000V. The output power is 500W and the output impedance is 20Ω
i) Find a power gain in decibels
ii) Find the voltage gain in decibels
iii) Find input impedance. (06 Marks)
b. Describe Miller's effect and derive an equation for Miller input and output capacitance. (06 Marks)
c. Discuss the effect of various capacitors on low-frequency response of BJT amplifier. (04 Marks)

OR

6 a. An amplifier rated 40W output is connected to a 10Ω speaker.
i) Calculate the input power required for full power output if the power gain is 25dB.
ii) Calculate the input voltage for rated output if the amplifier voltage gain 40dB. (04 Marks)
b. Determine the high-cutoff frequencies of JFET amplifier for the following specification:

$C_G = 0.01\mu F$, $C_C = 0.5\mu F$, $C_S = 2\mu F$,
$R_{sig} = 10\ K\Omega$, $R_G = 1m\Omega$, $R_D = 4.7K\Omega$, $R_S = 1K\Omega$, $R_L = 2.2K\Omega$,
$I_{DSS} = 8mA$, $V_P = -4V$, $r_d = \infty\Omega$, $V_{DD} = 20V$,
$C_{gd} = 2\ PF$, $C_{gs} = 4\ PF$, $C_{ds} = 0.5\ PF$, $C_{wi} = 5\ PF$, $C_{wo} = 6\ PF$ and $A_V = -3$. (06 Marks)

c. Explain the effect of multistage frequency of an amplifier. (06 Marks)

Module-4

7 a. Mention the types of feedback connections. Draw their block diagrams indicating input and output signal. (08 Marks)
b. With a neat circuit diagram, explain the working principle of FET phase–shift oscillator, with relevant equations. (08 Marks)

OR

8 a. What are the effects of negative feedback in an amplifier? Show how bandwidth of an amplifier increases with negative feedback. (06 Marks)
b. With a neat circuit and waveforms, explain the working operation of UJT relaxation oscillator. (05 Marks)
c. Determine the voltage gain, input and output impedance with feedback for voltage – series feedback having $A = -100$, $R_i = 10\ K\Omega$ and $R_0 = 20\ k\Omega$ for feedback factor $\beta = -0.1$. (05 Marks)

Module-5

9 a. With a neat circuit diagram, explain the operation of a series –fed class A power amplifier and prove that $\eta = 25\%$. **(08 Marks)**

b. Calculate the output voltage and the zener current in the regulator circuit of Fig.Q9(b) with $R_L = 1K\Omega$. **(04 Marks)**

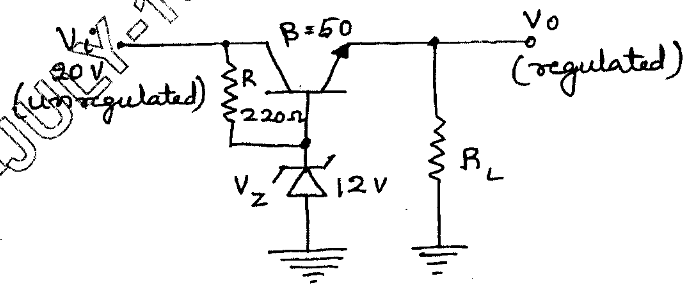

Fig.Q9(b)

c. Calculate the harmonic distortion components for an output signal with fundamental amplitude of 2.5V, second harmonic amplitude of 0.25, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05V. Also find total harmonic distortion. **(04 Marks)**

OR

10 a. Explain the operation of a transformer coupled, push-pull class –B amplifier and derive its conversion efficiency. **(07 Marks)**

b. Explain the fold –back current limiting circuit of voltage series regulator. **(05 Marks)**

c. Determine the regulated voltage and currents of shunt regulation of Fig.Q10(C). **(04 Marks)**

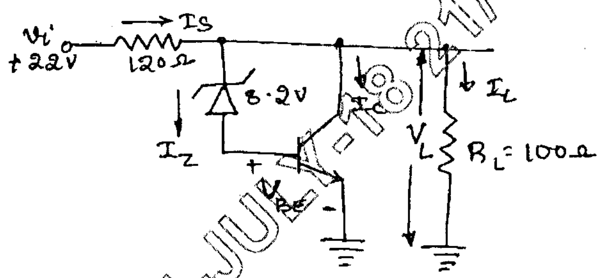

Fig.Q10(c)

* * * * *